74LVT244A; 74LVTH244A

3.3 V octal buffer/line driver; 3-state

Rev. 03 — 15 March 2006 Product data sheet

1. General description

The 74LVT244A; 74LVTH244A is a high-performance BiCMOS product designed for V_{CC} operation at 3.3 V.

This device is an octal buffer that is ideal for driving bus lines. The device features two output enables ($1\overline{OE}$, $2\overline{OE}$), each controlling four of the 3-state outputs.

2. Features

- Octal bus interface
- 3-state buffers
- Output capability: +64 mA and −32 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus hold data inputs eliminate need for external pull-up resistors to hold unused inputs
- Power-up 3-state
- Live insertion and extraction permitted
- No bus current loading when output is tied to 5 V bus
- Latch-up protection:
  - JESD78: exceeds 500 mA
- ESD protection:
  - HBM EIA/JESD22-A114-C exceeds 2000 V
  - MM EIA/JESD22-A115-A 200 V

3. Quick reference data

Table 1. Quick reference data

GND = 0 V; T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PLH}	LOW-to-HIGH propagation delay nAn to nYn	C_L = 50 pF; V_{CC} = 3.3 V	-	2.5	-	ns
t_{PHL}	HIGH-to-LOW propagation delay nAn to nYn	C_L = 50 pF; V_{CC} = 3.3 V	-	2.6	-	ns
C_i	input capacitance	V_I = 0 V or 3.0 V	-	4	-	pF
C_o	output capacitance	outputs disabled; V_O = 0 V or 3.0 V	-	8	-	pF
I_{CC}	quiescent supply current	outputs disabled; V_{CC} = 3.6 V; I_O = 0 A; V_I = GND or V_{CC}	-	0.13	-	mA

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4. Ordering information

Table 2. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVT244AD	–40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74LVT244ADB	–40 °C to +85 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74LVT244APW	–40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74LVTH244AD	–40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74LVTH244ADB	–40 °C to +85 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74LVTH244APW	–40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

5. Functional diagram

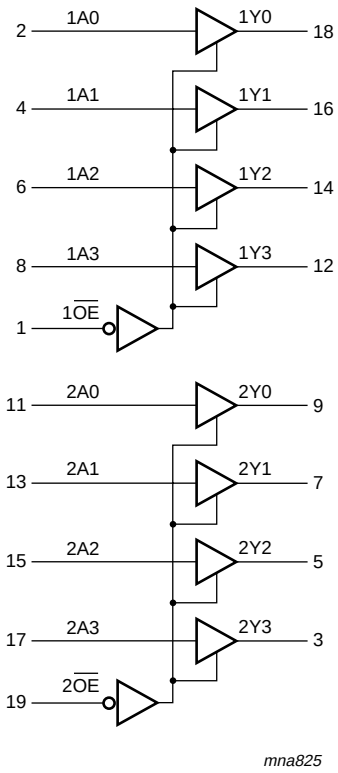


Fig 1. Logic symbol

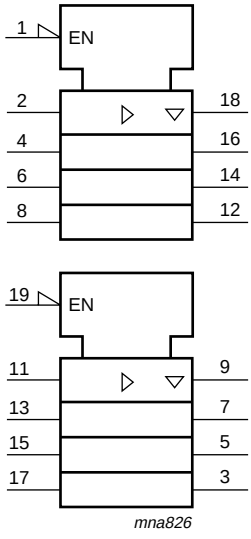


Fig 2. IEC logic symbol

6. Pinning information

6.1 Pinning

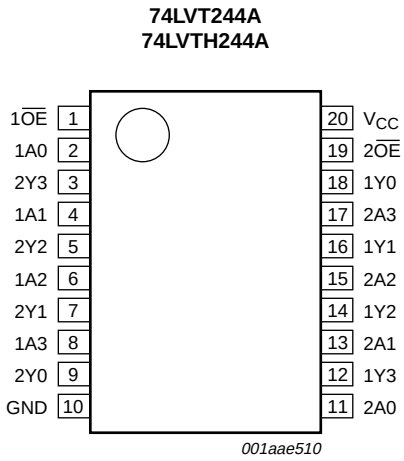


Fig 3. Pin configuration

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
$1\overline{OE}$	1	1 output enable input
1A0	2	1 data input 0
2Y3	3	2 data output 3
1A1	4	1 data input 1
2Y2	5	2 data output 2
1A2	6	1 data input 2
2Y1	7	2 data output 1
1A3	8	1 data input 3
2Y0	9	2 data output 0
GND	10	ground (0 V)
2A0	11	2 data input 0
1Y3	12	1 data output 3
2A1	13	2 data input 1
1Y2	14	1 data output 2
2A2	15	2 data input 2
1Y1	16	1 data output 1
2A3	17	2 data input 3
1Y0	18	1 data output 0
$2\overline{OE}$	19	2 output enable input
V_{CC}	20	supply voltage

7. Functional description

7.1 Function table

Table 4. Function table [1]

Control	Input	Output
$n\overline{OE}$	nAn	nYn
L	L	L
	H	H
H	X	Z

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care;
Z = high-impedance OFF-state.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+4.6	V
V_I	input voltage		[1]	–0.5	+7.0	V
V_O	output voltage	output in OFF-state or HIGH-state	[1]	–0.5	+7.0	V
I_{IK}	input clamping current	$V_I < 0$ V		-	–50	mA
I_{OK}	output clamping current	$V_O < 0$ V		-	–50	mA
I_O	output current	output in LOW-state		-	128	mA
		output in HIGH-state		-	–64	mA
T_{stg}	storage temperature			–65	+150	°C
T_j	junction temperature		[2]	-	150	°C

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

9. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.7	-	3.6	V
V_I	input voltage		0	-	5.5	V
V_{IH}	HIGH-state input voltage		2.0	-	-	V
V_{IL}	LOW-state input voltage		-	-	0.8	V

Table 6. Operating conditions *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{OH}	HIGH-state output current		-	-	–32	mA
I_{OL}	LOW-state output current	none	-	-	32	mA
		current duty cycle ≤ 50 %; $f_i \geq 1$ kHz	-	-	64	mA
T_{amb}	ambient temperature	in free-air	–40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	outputs enabled	-	-	10	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = –40 °C to +85 °C [1]							
V_{IK}	input clamping voltage	V_{CC} = 2.7 V; I_{IK} = –18 mA		-	–0.9	–1.2	V
V_{OH}	HIGH-state output voltage	V_{CC} = 2.7 V to 3.6 V					
		I_{OH} = –100 µA		V_{CC} – 0.2	V_{CC} – 0.1	-	V
		I_{OH} = –8 mA		2.4	2.5	-	V
		V_{CC} = 3.0 V					
		I_{OH} = –32 mA		2.0	2.2	-	V
V_{OL}	LOW-state output voltage	V_{CC} = 2.7 V					
		I_{OL} = 100 µA		-	0.1	0.2	V
		I_{OL} = 24 mA		-	0.3	0.5	V
		V_{CC} = 3.0 V					
		I_{OL} = 16 mA		-	0.25	0.4	V
		I_{OL} = 32 mA		-	0.3	0.5	V
		I_{OL} = 64 mA		-	0.4	0.55	V
I_{LI}	input leakage current						
	all input pins	V_{CC} = 0 V or 3.6 V; V_I = 5.5 V		-	0.1	10	µA
	control pins	V_{CC} = 3.6 V; V_I = V_{CC} or GND		-	±0.1	±1	µA
	data pins	V_{CC} = 3.6 V	[2]				
		V_I = V_{CC}		-	0.1	1	µA
		V_I = 0 V		-	–1	–5	µA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or V_O = 0 V to 4.5 V		-	1	±100	µA
I_{HOLD}	bus hold current A input	V_{CC} = 3 V	[3]				
		V_I = 0.8 V		75	150	-	µA
		V_I = 2.0 V		–75	–150	-	µA
		V_{CC} = 0 V to 3.6 V					
		V_I = 3.6 V		±500	-	-	µA
I_{EX}	external current into output	output in HIGH-state when $V_O > V_{CC}$; V_O = 5.5 V; V_{CC} = 3.0 V		-	60	125	µA

Table 7. Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{O(pu/pd)}$	power-up/power-down output current	$V_{CC} \leq 1.2$ V; $V_O = 0.5$ V to V_{CC}; V_I = GND or V_{CC}; n$\overline{OE}$ = don't care	[4]	-	±1	±100	µA
I_{OZ}	OFF-state output current	$V_{CC} = 3.6$ V; $V_I = V_{IH}$ or V_{IL}					
		output HIGH: $V_O = 3.0$ V		-	1	5	µA
		output LOW: $V_O = 0.5$ V		-	–1	–5	µA
I_{CC}	quiescent supply current	$V_{CC} = 3.6$ V; V_I = GND or V_{CC}; $I_O = 0$ A					
		output HIGH		-	0.13	0.19	mA
		output LOW		-	3	12	mA
		outputs disabled	[5]	-	0.13	0.19	mA
ΔI_{CC}	additional quiescent supply current	per input pin; $V_{CC} = 3.0$ V to 3.6 V; one input at $V_{CC} - 0.6$ V and other inputs at V_{CC} or GND	[6]	-	0.1	0.2	mA
C_i	input capacitance	$V_I = 0$ V or 3.0 V		-	4	-	pF
C_o	output capacitance	outputs disabled; $V_O = 0$ V or 3.0 V		-	8	-	pF

[1] All typical values are at $T_{amb} = 25$ °C.

[2] Unused pins at V_{CC} or GND.

[3] This is the bus hold overdrive current required to force the input to the opposite logic state.

[4] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms. From $V_{CC} = 1.2$ V to $V_{CC} = 3.3$ V ± 0.3 V a transition time of 100 µs is permitted. This parameter is valid for $T_{amb} = 25$ °C only.

[5] I_{CC} is measured with outputs pulled to V_{CC} or GND.

[6] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 6.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = -40$ °C to +85 °C [1]						
t_{PLH}	LOW-to-HIGH propagation delay nAn to nYn	see Figure 4				
		$V_{CC} = 2.7$ V	-	-	5.0	ns
		$V_{CC} = 3.0$ V to 3.6 V	1	2.5	4.1	ns
t_{PHL}	HIGH-to-LOW propagation delay nAn to nYn	see Figure 4				
		$V_{CC} = 2.7$ V	-	-	5.1	ns
		$V_{CC} = 3.0$ V to 3.6 V	1	2.6	4.1	ns
t_{PZH}	output enable time to HIGH-level	see Figure 5				
		$V_{CC} = 2.7$ V	-	-	6.3	ns
		$V_{CC} = 3.0$ V to 3.6 V	1	3.2	5.2	ns
t_{PZL}	output enable time to LOW-level	see Figure 5				
		$V_{CC} = 2.7$ V	-	-	6.7	ns
		$V_{CC} = 3.0$ V to 3.6 V	1.1	3.1	5.2	ns

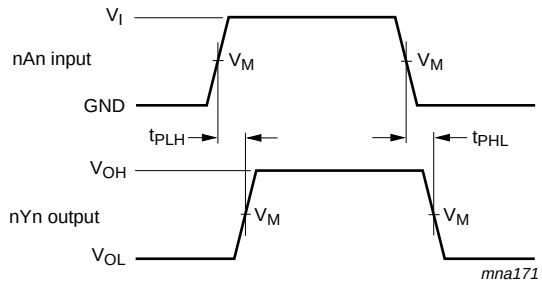
Table 8. Dynamic characteristics *…continued*

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 6.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PHZ}	output disable time from HIGH-level	see Figure 5				
		V_{CC} = 2.7 V	-	-	6.3	ns
		V_{CC} = 3.0 V to 3.6 V	1.9	3.3	5.6	ns
t_{PLZ}	output disable time from LOW-level	see Figure 5				
		V_{CC} = 2.7 V	-	-	5.6	ns
		V_{CC} = 3.0 V to 3.6 V	1.8	3.3	5.1	ns

[1] All typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.

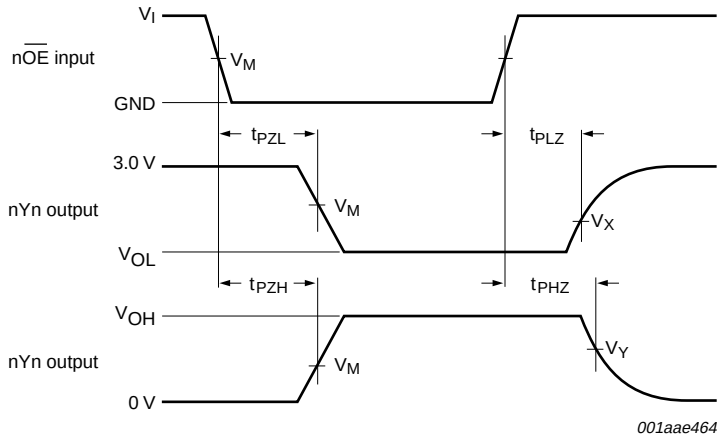
12. Waveforms



Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

Fig 4. Propagation delay input (nAn) to output (nYn) propagation delays



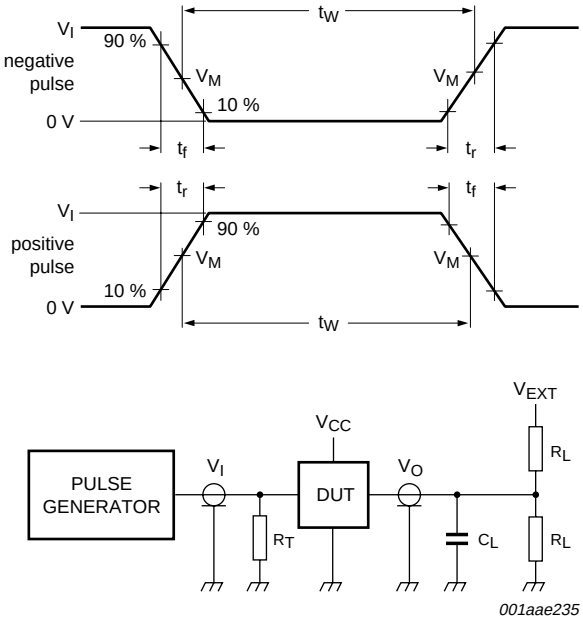
Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

Fig 5. 3-state output enable and disable times

Table 9. Measurement points

Input	Output		
V_M	V_M	V_X	V_Y
1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} – 0.3 V



Test data is given in Table 10.

Definitions test circuit:

R_L = Load resistor.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = Test voltage for switching times.

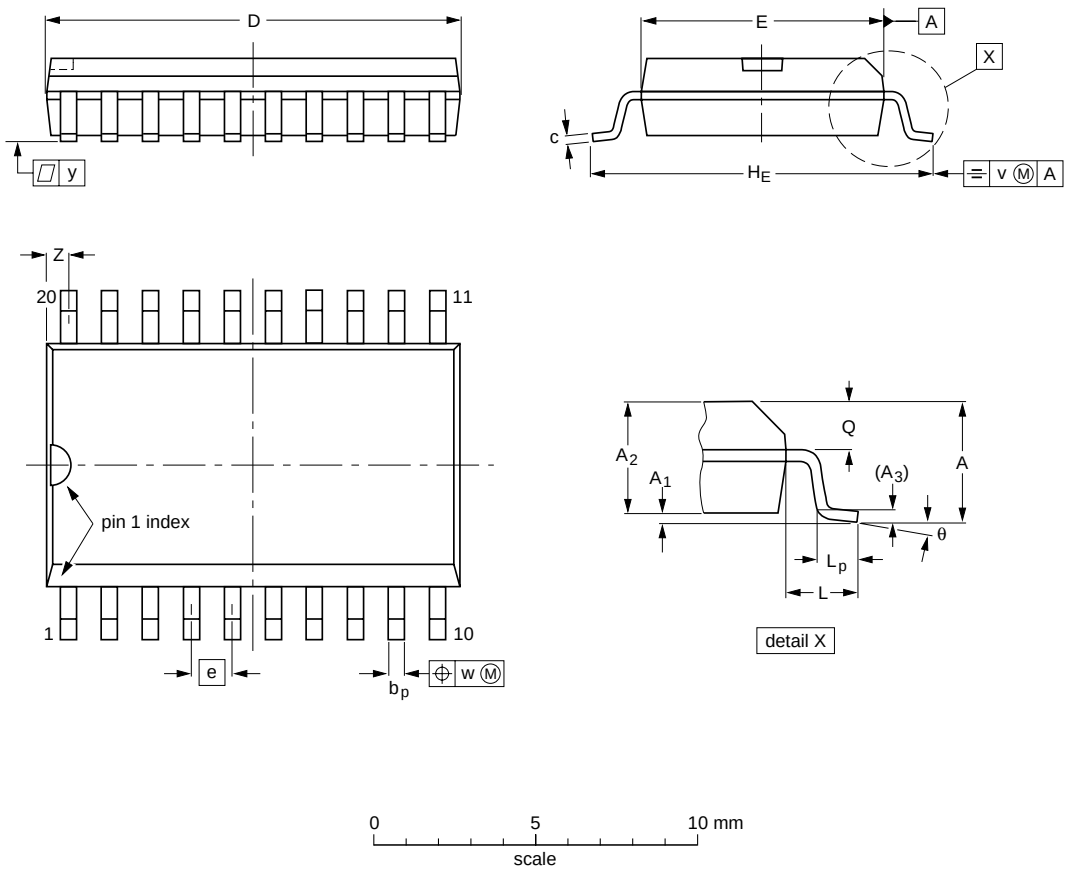
Fig 6. Load circuitry for switching times

Table 10. Test data

Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r, t_f	C_L	R_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	GND	6 V	open

13. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

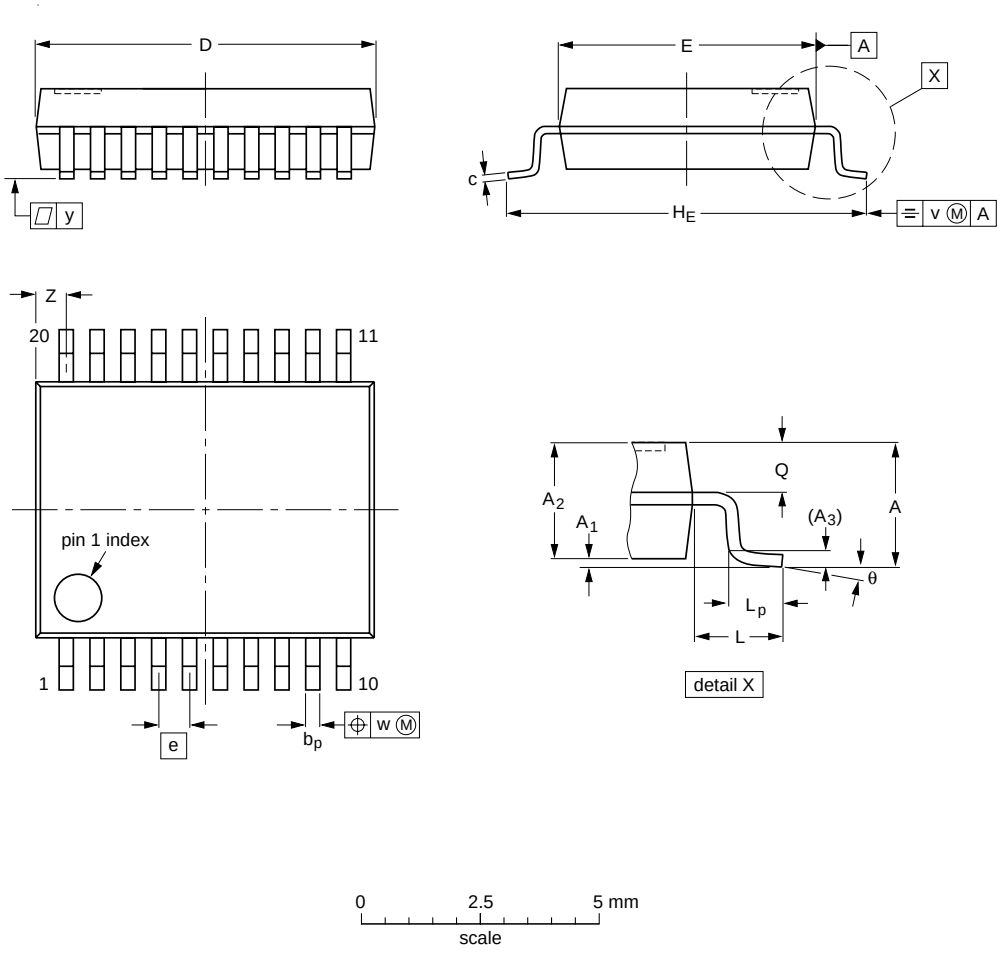
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Fig 7. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm **SOT339-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8^o 0^o

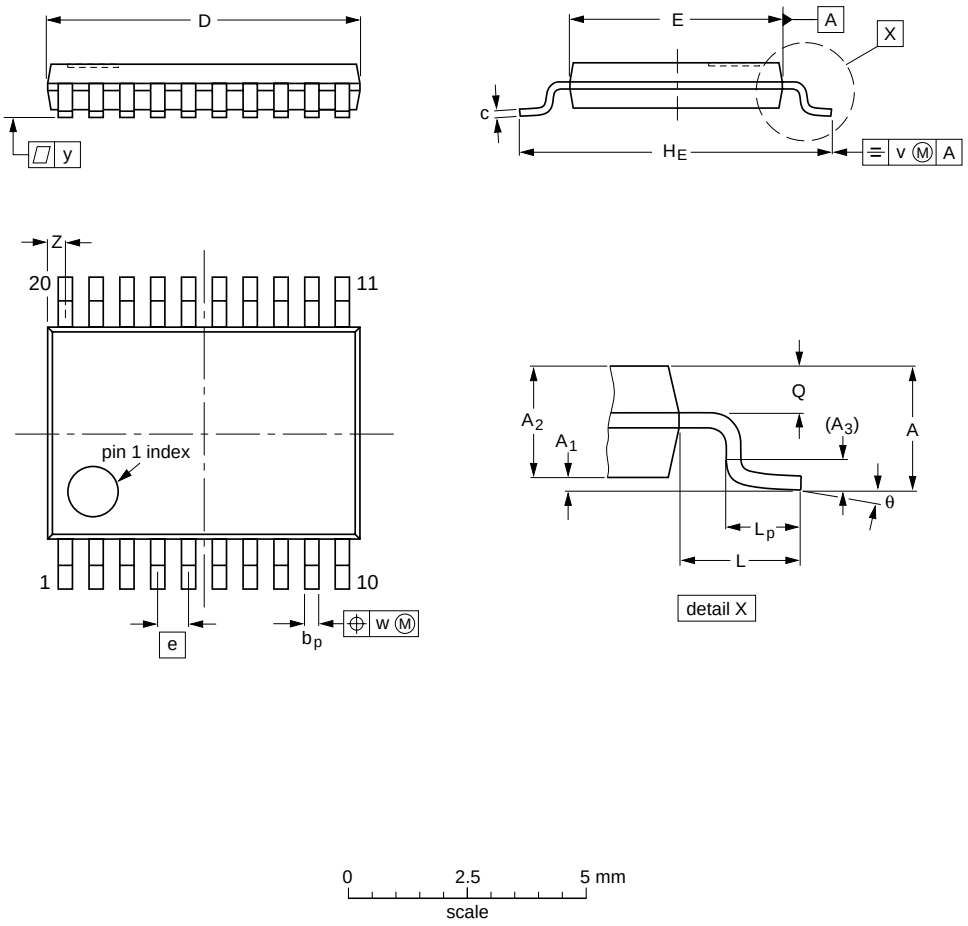
Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT339-1		MO-150				~~99-12-27~~ 03-02-19

Fig 8. Package outline SOT339-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Fig 9. Package outline SOT360-1 (TSSOP20)

14. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT_LVTH244A_3	20060315	Product data sheet	-	74LVT244A_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. • Section 4: added type numbers 74LVTH244AD, 74LVTH244ADB and 74LVTH244APW.			
74LVT244A_2	19980219	Product specification	-	74LVT244A_1
74LVT244A_1	19951114	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.semiconductors.philips.com.

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